B4 6H O@ J8

%O!<%I%&%'%"5-=R8@8lKh$k
FPGA >eXN
6 50 iMQ%^%$%/%m%W%m%;%C%5$N<BAu

;a L> !'EDCf 5A5W
3X@RHV9f !'2210940211-0
;XF3 65 0w !';3:j>!90
Ds =P F| !'1998 G/2 7n20 F|

N)L?4[Bg3XM}9)3XIt>pJs3X2J

FbMF9<35

%O!<%I%&%'%"$H%=%U%H%&%'%"$+iJ$k!$FOD jMQES8~1N%7%9%F%`$r3+H/$9$k<jK!$H$7$F!$!VO!<%I%&%'%"/%=%U%H%&%'%"!&3%G%6%$%s!W$,CmL\$5$l$k$h$&$K$J$C$F$-$F$$$k!%$3$l$O!$%O!<%I%&%'%"@_7W$H%=%U%H%&%'%"@_7W$r!$8_$$$K9MN8$7$J$,$iF1;~$K9T$C$F$$$/@_7W<jK!$G$"$k!%HW/SW %3%G%6%$%s$N:G=*L\I8$O!$%7%9%F%`A4BN$rE}0lE*$K%b%G%k2=$7!$@)Ls$K4p$E$$$F%O!<%I%&%'%"ItJ,$H%=%U%H%&%'%"ItJ,$rJ,3d$7!$$5iK%O!<%I%&%'%"$H%=%U%H%&%'%"$r<+F0@8@.9k3HG"$k!%$7$+$7J,$i!$$$$^$@$K<BMQKO$$$?CF$$$J$$$N$,8=>u$G$"$k!%

HW/SW %3%G%6%$%s$N8&5fKO!$CPU $NFbIt9=B$$N>\:Y5Z$S%O!<%I%&%'%"5-=R8@8l!&FPGA $NM}2r$,IT2D7gHNG'<1$+$i!$K\8&5f$G$O!VKITE %^%$%/%m%W%m%;%C%5!W$N<B8=J}K!$K$D$$$F=R$Y!$%O!<%I%&%'%"5-=R8@8l(VHDL) $rMQ$$$F KITE CPU $N@_7W$r9T$&!%$^$?!$FPGA $rEk:\$9$k!VKITE %^%$%/%m%W%m%;%C%5!&%\!<%I!W$rMQ$$$FF0:n8!>Z$r9T$&!%KITE %^%$%/%m%W%m%;%C%5$O!$KITE %\!<%IMQ$K@_7W5l$?650iMQ CPU G"$j!$@_7W!&B Au$r9MN8$7$?4JC1$J%"!<%-%F%/%A%c9=@.HJCF$*$j!$K\8&5f$NL\E*$KE,7F$$$k!%

7k2LH7$F!$CPU $O40@.$K$O;j$C$F$$$J$$$,!$FPGA >e$G!V?Na8l$N%U%'%C%A"*%G%3!<%I"*(8Bil$?) L?Na$N<B9T!W$H$$$C$?CPU $N4pK\F0:n$r9T$&$bN,40@.7?!%FPGA >eGNF0:n8!>Z$GH/8+$5l?LdBjE@JI$r9nI~$9k3HKhC$F!$CPU @_7W$N%N%&%O%&$r2qF@G-!$VHDL $H FPGA $NM}2r$H$$$&L\E*$bC#@.$5l?$H;W$olk!%

L\<!

1 O8aK

6aG/!$7HBSEEOC$dEE;R<jD"!$%F%l%S$JIN5^6^$JEE2=@=I$J$K!V3%s%T%e!<%?!W$,AH $_9~$^lkh&KJCF$-$F$$$k!%$=$7F3li$N%3%s%T%e!<%?$O CPU!$RAM!$%W%m%0 %i%`$r<}$a$?ROM $J$I$+$i9=@.$5$l!$$"$k$$$O$=$l$iA4$F$,%o%s%A%C%W$G<B8=$5$l!$0l $D$N%3%s%T%e!<%?!&7%9%F%`$r9=@.$7$F$$$k!%

7+$7!$$=li$N%7%9%F%`$,%Q%=%3%s$J$I$N0lHLE*$J%3%s%T%e!<%?%7%9%F%`$H0[JkE@ $O!$8Bil$?FCDjMQES8~$1G"$k;v$H!$$"$k0lDj$N@)Ls$,IU$/;vG"$k!%Nc$($P!$%G%8%? %k7HBSEEOC$N>l9g!$2;@<%G!<%?$r%j%"%k%?%$%`$G=hM}$9$k$?$a!$$"$kDxEY$N=hM}G=NO$,$J $1$l$P$J$i$J$$!%$7$+$7!$2TF/;~4V$r?-$P$9$?$a$K!$CPU $N>CHqEENO$rM^$($J$1$l$P$J$i $J$$!%$5$i$K!$@=IJ%3%9%H$rM^$($k$?$a$K!$CPU $N%3%9%H$bM^$($J$1$l$P$J$i$J$$!%$3$N $h$&$J@)Ls$K8+9g$C$?%7%9%F%`$r:n$kKO!Nc($P<!$Nh&$J<jK!$r<h$k!%9b$$=hM}G=NO $,I,MW$JItJ,$O!$$=$N=hM}$r%O!<%I%&%'%"$G<B8=$7$F9bB.2=$7!$9b$$=hM}G=NO$,I,MW$G$J $$ItJ,$O!$$=$N=hM}$r%=%U%H%&%'%"$G<B8=$9$k;v$KhC$F!$%7%9%F%`$N%3%9%H$r2<2k;v $,$G$-$k!%5i$K!$$3li$N@)Ls$d3+H/4|4V$N:GE,2=$N$?$aKO!$%O!<%I%&%'%"$N@_7W$H %=%U%H%&%'%"$N@_7W$r!$8_$$$K9MN8$7$J$,$iF1;~$K9T$C$F$$$/I,MW$,$"$k!%

3Nh&$J%7%9%F%`@_7W<jK!$O!$%O!<%I%&%'%"/%=%U%H%&%'%"!&%3%G%6%$%s!W(0J2<HW/SW %3%G%6%$%s$HN,$9) $H8F$P$l!$=>Mh$+$i=ON}$N@_7W<T$K$h$C$F9T$o$l$F$-$?!%$7$+$7:G6a!$ 7W;;5!$,9b@-G=2=$7!$7W;;5!>e$G$NO@M}9g@.$d%7%_%e%l!<%7%g%s$N5;=Q$N?JJb$G!$HW/SW %3%G%6%$%s$N$?$a$N CAD 4D6-$,@0$C$F$-$F$*$j!$$^$?!$%W%m%0%i%`2DG=$J%O!<%I%&%'%" (FPGA) $,EP>l$7!$%O!<%I%&%'%"ItJ,$N8!>Z$,MF0W$KJjDD$"$kJI$NM}M3$Khj!$ HW/SW %3%G%6%$%s$,CmL\$5lkh&KJCF$-$F$$$k[7]!%

8=:_$N HW/SW %3%G%6%$%s$N:G=*E*$JL\I8$O!$%7%9%F%`A4BN$rE}0lE*$K%b%G%k2=$7!$@) Ls$K4p$E$$$F%O!<%I%&%'%"ItJ,$H%=%U%H%&%'%"ItJ,$rJ,3d$7!$$5$i$K%O!<%I%&%'%"$H%=%U %H%&%'%"$r<+F0@8@.$9$k$3$H$G$"$k!%$7$+$7$J$,$i!$HW/SW %3%G%6%$%s$K4X$9$k8&5f$O Hs>o$KKDBg$G!$%O!<%I%&%'%"!&%=%U%H%&%'%":.:_%7%9%F%`$r8zN(E*$K5-=RG-$k8@8l$N3+ H/!$5-=R$5l?%7%9%F%`$N5!G=8!>Z$r9T$&5;=Q!$%7%9%F%`5-=R$+$i%O!<%I%&%'%"ItJ,HH %=%U%H%&%'%"ItJ,$r<+F0E*$KJ,N%!&J,3d9k5;=Q!$%O!<%I%&%'%"$N%3%9%H!&@-G=!&>CHqEE NOJI$r@53N$K8+@Qbk5;=Q!$J,N%$5l?5-=R$+$i%O!<%I%&%'%"5Z$S%=%U%H%&%'%"$r<+F0 @8@.9k5;=Q!$$J$ILLdBj$O;3@Q$_$G$"$j!$$7$+$b$=$NIlb,:,K\E*$J2r7h$K;jCF$$$J $$$N$,8=>u$G$"$k[7, 8]!%

K\8&5fGO!$HW/SW %3%G%6%$%s$NBh0lJb$H7F!$%O!<%I%&%'%"5-=R8@8l$rMQ$$$F%^%$ %/%m%W%m%;%C%5$r@_7W$7!$$^$?$=$N%^%$%/%m%W%m%;%C%5$r FPGA >e$GF0:n5;$k;v$rL\E* H9$k!%F0:n8!>Z$K$O!$KITE %^%$%/%m%W%m%;%C%5%\!<%I!W(0J2<KITE %\!<%I)$r;HMQ 9k!%KITE %\!<%I$O!$DL>o$N CPU NBeojN%G%P%$%9$H7F FPGA $,Ek:\$5lF$$$k %\!<%I%3%s%T%e!<%?G"$k[3]!%

@_7W9k CPU $O!KITE-I %^%$%/%m%W%m%;%C%5!W(0J2<KITE CPU)H9$k!%KITE CPU $O LSI $N@_7W650i$rL\E*$K3+H/$5l?CPU G"kN$G!$@_7W!&BAu$r9MN8$7$?4JC1 $J%"!<%-%F%/%A%c9=@.$HJCF*$j[4]!$K\8&5f$NL\E*$KE,7F$$$k!%$^$?!$4{B8$N CPU $HF1$8 CPU $r:n@.$9lP!$$=li$rHf3S$9k3HKhC$F!$F0:n8!>Z$,MF0W$KJk!$$J

INMxE@$,$"$k!%

:G=i$KBh 2 >O$G$O!$HW/SW %3%G%6%$%s$N35MWKD$$$F=RYk!%Bh 3 >OGO!$3+H/BP>] H9$k KITE %^%$%/%m%W%m%;%C%5$N;EMMKD$$$F=RYk!%5i$KBh 4 >O$G$O!$%^%$%/%m%W %m%;%C%5$NFbIt9=B$$N>\:YKD$$$F=RYk!%Bh 5 >OGO!$3+H/$7$?%^%$%/%m%W%m%;%C%5$N @5Ev@-$r3NG'9k$?$a$N8!>ZJ}K!5Z$S8!>Z7k2L$r=R$Y$k!%Bh 6 >O$G$O!$8=:_$^$G$N@.2L$H :#8e$N2]Bj$r=RYk!%

2 %O!<%I%&%'%"/%=%U%H%&%'%" %3%G%6%$%s

2.1 %O!<%I%&%'%"/%=%U%H%&%'%" %3%G%6%$%s$N8=>u

HW/SW %3%G%6%$%s$N:G=*E*$JL\I8$O!$%O!<%I%&%'%"$H%=%U%H%&%'%"$N:.:_%7%9%F%`$rE}0lE*$K5-=R$7!$$=lr@)Ls>r7o$K4p$E$$$F%O!<%I%&%'%"ItJ,$H%=%U%H%&%'%"ItJ,$H$KJ,N%$7!$$5iK%O!<%I%&%'%"$H%=%U%H%&%'%"$r<+F0@8@.9k3HG"$k[7]!%$7$+$7J,$i!$$3$NJ}K!$O!$%O!<%I%&%'%"$H%=%U%H%&%'%"$NN>J}$,2DJQG"k?$a!$LdBj$,J#;($G2r7h$,:$FqG"$k!%

7?$,$C$F!$8=:_$N HW/SW %3%G%6%$%s$O!$<g$K%7%9%F%`$N0lIt$r8GDj2=$7!$LdBj2r7h$r?^jd9/7?J}K!GN8&5f$,9T$olF$$$k!%8=:_$N HW/SW %3%G%6%$%s$N8&5f$O!$<g$K<!$N2 DKBgJL5l$k[7, 8]!%

1. 4{B8$N CPU %3%"$rN.MQ9kJ}K!
   3l$O!$%7%9%F%`$r4{B8$N CPU H=$N CPU >e$GF0:n9k %=%U%H%&%'%"H7$F<B8=$7!$%=%U%H%&%'%"ItJ,$N%\%H%k%M%C%/HJCF$$$kItJ,$r!$@lMQ%O!<%I%&%'%"$G<B8=$9k3HG9bB.2=$r?^$kJ}K!G"$k!%

2. CPU $N%3%"$b2DJQH9$kJ}K!
   3l$O!$CPU $NL?Na%;%C%H%"!<%-%F%/%A%cJI$O8GDj2=$7F7$^$$!$%G!<%?%S%C%HI}!&"%I%l%9%S%C%HI}!&%l%8%9%??t!&ALU ?tJI$O!$%W%m%0%i%`$K$"$o$;$F7hDj$7!$%A%C%W$NO@M}%2!<%H?t$d>CHqEENO$J$I$r:GE,2=$9$k<jK!$G$"$k!%CPU, RAM, ROM $J$I$r%o%s%A%C%W$K<}$a$k%7%9%F%`$GM-8z$J<jK!G"$k!%

2.2 %O!<%I%&%'%"5-=R8@8l VHDL

%O!<%I%&%'%"5-=R8@8l(HDL) HO!$2sO)$NF0:n$d9=B$$r5-=R9k8@8lG"$k!%=>Mh$N%G%8%?%k2sO)$O!$2sO)?^$r;HMQ$7$F@_7W$,J5lF$-$?$,!$HDL GO!$O@M}%2!<%H%l%Y%k$h$jC:j>]EY$N9b$$%l%Y%k$G5-=R$G$-$kNG!$%V!<%kBe?t<0$r9M$($k<j4V$,>J$1!$3+H/4|4V$,C;=LG-!$$h$jBg5,LO$J2sO)$r@_7W$7d9$/$J$k!%$7$?$,CF!$6aG/$N2sO)$NBg5,LO2=$KH<$$!$2sO)?^$rMQ$$$kJ}K!$+$i!$%O!<%I%&%'%"5-=R8@8l!W$*hS !2sO)%7%_%e%l!<%?!W$!V@M}9g@.%D!<%k!W$rMQ$$$?@_7W$KO\9T$DD"$k[9]!%

7+7J$,$i!$HDL %3%s%Q%$%i$,O@M}9g@.$7$?2sO)$O!$?M4V$,%2!<%H%l%Y%k$G@_7W$7$?2sO)$hjb5,LO$,Bg$-$/$J$k>l9g$,B?$$!$$H$$$&7gE@$,$"$k!%

HDL KO!$0J2<$Nh&$K$$$/D+$N<oN`$,$"$k[9]!%

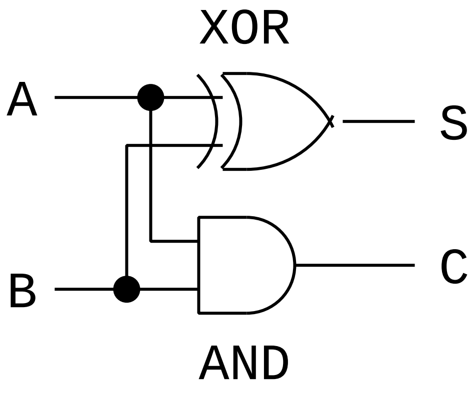
- VHDL
  9b$$%7%9%F%`5-=RG=NO$KFCD'$,$"$k!%V@M}9g@.!W$rL\E*$H$7$?2sO)F0:n5-=R$@$1$G$J$/!$%7%9%F%`F0:n$N%7%_%e%l!<%7%g%s$b5-=R2DG=G"$k!%
- Verilog-HDL
  F|K\9qFb5Z$SJF9q$G$O VHDL hjI a5Z7F$$$k!%%7%9%F%`5-=RG=NO$O VHDL $[$I9b$/$J$$!%

- SFL (Structured Function description Language)
  NTT $,3+H/$7$?PARTHENON (%Q%k%F%N%s) %7%9%F%`$,M-L>!%
- UDL/I (Unified Design Language for Integrated circuit)
  F|K\EE;R9)6H?66=6(2q$,3+H/$7!$1996 G/2 7n$K%U%j!<!&=%U%H%&%'%"H7$F0lHL$K8x3+5l$?!%

Hjo1 VHDL $O%7%9%F%`5-=RG=NO$,M%lF$*$j!$B>$N8@8lKHfY!$<!$Nh&$JMxE@$,$"$k!%[9, 10]

- VHDL $O!$O@M}%2!<%H%l%Y%k$+$i%G!<%?%U%m!<5-=R!&F0:n5-=R$^$G$NI}9-$$!V%j>]2=%l%Y%k!W$r%5%]!<%H$7$F$$$k!%
- VHDL $O%7%_%e%l!<%7%g%s$N$?$a$N5-=R$,Hs>o$K:Y$+$/Dj5A$5lF$$$k$?$a!$@53N$J2sO)%7%_%e%l!<%7%g%s$,2DG=$G$"$k!%$^$?!$2sO)%7%_%e%l!<%7%g%s$N$?$a$N%W%m%0%i%`(!V%F%9%H%Y%s%A!W$H$$$&) $b VHDL $G5-=R$G$-$k!%
- VHDL $O IEEE 5Z$S ANSI $NI8=`5,3J$G$"$kNG!$VHDL $G5-=R$5l?%b%G%k$O0\?"@-$,$"$k!%

NcH7$F!$?^1Nh$&$JH>2C;;4o$N VHDL 5-=R$O!$?^2$Nh&KJ$k!%VHDL GO!$1i;;;R "+" "-" "*" $rMQ$$$k3H$G!$2C;;4oJI$r<+F0@8@.$9kN$G!$A42C;;4oJI$O?^3$Nh&$KHs>o$K4J7i$K!$9b$$Cj>]EY%l%Y%k$G5-=R$G$-$k!%J*!$"--" 0J9_$O%3%a%s%H$_$J5l!$L5;k$5lk!%



?^1: H>2C;;4o$NO@M}2sO)?^

?^2K*$$$F!$1-6 9TL\$^GO%(%s%F%#%F%#@k8@$H8F$P$l!$%b%G%k2=5l$kO@M}2sO)$NL>A0 (HalfAdder) $H!$B>$NO@M}2sO)$H?.9frd$j<h$j9k$?$a$N%]!<%H$rDj5A9k!%3 9TL\$O 1bit $N?.9f$rdj<hj9$k A $H B $H$$$&%]!<%H$rDj5A$7!$$=li$,F~NO$H7F;HMQ5l$k!%4 9TL\$G$OF1$8h&$K!$C $H S $,=PNOMQ%]!<%H$H7FDj5A5l$k!%

```
 1 : entity HalfAdder is                -- O@M}2sO)L>$rDj5A
 2 :    port(
 3 :       A, B : in  std_logic;        -- F~NO?.9f A, B $rDj5A
 4 :       C, S : out std_logic         -- =PNO?.9f C, S $rDj5A
 5 :    );
 6 : end HalfAdder;
 7 :
 8 : architecture RTL of HalfAdder is   -- HalfAdder $N9=B$$rDj5A
 9 : begin
10 :    C <= A or  B;                   -- C $K A or B $N7k2L$rBeF~
11 :    S <= A xor B;                   -- S $K A xor B $N7k2L$rBeF~
12 : end RTL;
```

?^2: H>2C;;4o$N VHDL Kh$k5-=R

```
 1 : entity FullAdder is                              -- O@M}2sO)L>$rDj5A
 2 :    port(
 3 :       A, B : in  std_logic_vector( 3 downto 0 ); -- 4bit $NF~NO?.9fA,B $rDj5A
 4 :       S    : out std_logic_vector( 3 downto 0 )  -- 4bit $N=PNO?.9f S $rDj5A
 5 :    );
 6 : end FullAdder;
 7 :
 8 : architecture RTL of FullAdder is                 -- FullAdder $N9=B$$rDj5A
 9 : begin
10 :    S <= A + B;                                   -- 4bit $N?.9f$N
11 : end RTL;                                         -- 2C;;$r9T$&
```

?^3: A42C;;4o$N "+" 1i;;R$Khk5-=R

8-12 9TL\$O%"!<%-%F%/%A%c@k8@$H8F$P$l!$HalfAdder $N<B:]$NF0:n$d9=B$$,5-=R5l$k!% 10 9TL\$G$O?.9f C $K A and B $N7k2L$,BeF~5l!$11 9TL\$G$O?.9f S $K A xor B $N7k2L $,BeF~$5lk!%

2.3 FPGA

FPGA (Field Programable Gate Array) $O!$FbItK"i+8a AND %2!<%H$d OR %2!<%H$r@_1F$*$-!$$=li$NFbIt@\B3$rEE5$E*$KJQ99$9$k3HKhCF!G0U$NO@M}2sO)$r<B8=9k LSI G"$k[10]!%

=>Mh!$@_7W$7$? LSI $NF0:n8!>Z$O!$<B:]$K%F%9%HMQ$N%A%C%W$r>F$/$+!$%7%_%e%l!<%7%g%s$KMjk7$+$J$+$C$?!%$7$+$7!$

- %A%C%W$r>F$/KO!$;~4V$H%3%9%H$,$+$+$k!%
- %7%_%e%l!<%7%g%s$O!$Bg5,LO$J LSI KO%7%_%e%l!<%7%g%sKMW9$k;~4V$,$+$+j9$.$k$?$a!$<BMQE*$GOJ$$!%

JI$NLdBj$,$"$k!%3liNLdBj$O FPGA $NEP>l$KhC$F2r7h$5l?!%@_7W7?LSI $N9=@.%G!<%?$r FPGA $K%m!<%I$9k3HKhj!$%N!<%3%9%H$G!$%7%_%e%l!<%7%g%s$hjbOk$+$K9bB.$KF0:n$5$;$k3H$,$G$-!$$9Pd$/F0:n8!>Z$,9T$($k!%9JoA!$$"$?$+$b%=%U%H%&%'%"$N3+H/$r9T$&h&$J4JJX$5$G!$LSI $N3+H/$r9T$&$3H,2DG=G"$k!%$3$NE@$K$*$$$F!$FPGA $N HW/SW %3%G%6%$%sKBP9$k9W8%EY$OBg$-$$!%

$^$?!$FPGA $rF0:n8!>Z$KMQ$$$k$@$1GJ$/!$%\%H%k%M%C%/HJCF$$$k%=%U%H%&%'%"ItJ,$r!$O@M}2sO)KCV-49$($F FPGA >e$G<B9T$5$;$k!W$H$$$C$?!$FPGA $r2DJQE*$J%3%W%m%;%C%5H7$FMQ$$$k8&5f$b9T$olF$$$k[7]!%

3 KITE %^%$%/%m%W%m%;%C%5

3.1 KITE %^%$%/%m%W%m%;%C%5 !&\!<%I

KITE %^%$%/%m%W%m%;%C%5 !&\!<%I[3] $O!$LSI $N@_7W650i$rL\E*$K3+H/$5l?%\!<%I%3%s%T%e!<%?G"$k!%KITE %\!<%I$K$O!$DL>o$N CPU NBeojN%G%P%$%9$H7F!$FPGA $,Ek:\$5lF$$$k!%FPGA $rL\E*$N LSI H7$FF0:n$5$;$k$?$a$N !%O!<%I%&%'%"9=@.%G!<%?!W$r!$FPGA $K%m!<%I$9k3HKhj!$FPGA $rFH<+$N LSI H7$F<B:]$KF0:n5;k3H,G-!$@_7W$+$i<BAu!&F0:n8!>Z$JIr9Pd/9T$($k$H$$$&FCD'$r;}$C$F$$$k!%$^$?!$KITE %\!<%I>e$K$OB?$/$N LED ?tCM%G%#%9%W%l%$!&LED %i%s%WJI$,Ek:\$5lF$*$j!$LSI $NFbIt>uBV$OFCJL$J%b%K%?!&W%m%0%i%`$JIr2p5:Hb4QB,2DG=G"$k!%

KITE %\!<%I>eKO!$FPGA $r KITE CPU H7$FF0:n5;k?aN9=@.%G!<%?$,$"i+8aMQ0U$5lF$*$j!$EE8;EjF~;~$K FPGA $K%m!<%I$9k3HKhj!$KITE %\!<%I$rDL>o$N%\!<%I%3%s%T%e!<%?$H7F;HMQ9k3H$b2DG=$G$"$k!%

I=1$K KITE %\!<%I$N<g$J;EMM$r=RYk!%

I=1: KITE %^%$%/%m%W%m%;%C%5%\!<%I ;EMM

CPU (FPGA)	XILINX XC4010
RAM	64K %o!<%I (128K %P%$%H)
4QB,MQI=< (4o	LED ?tCM%G%#%9%W%l%$:28 8D LED %i%s%W:26 8D
%/%m%C%/	0.1Hz ∼ 1MHz @ZjBX(<jF0Kh$k%/%m%C%/A*Br2DG=

KITE %\!<%IMQ$N%/%m%9%=%U%H%&%'%"$H7F!$C %3%s%Q%$%i (KITE CPU MQ) !$%"%;%s%V%i (KITE CPU MQ) !$%?!<%_%J%k%=%U%H (%[%9%H%3%s%T%e!<%?$+$i KITE %\!<%I$N%a%b%j$K%"%/%;%9$9$k!%%W%m%0%i%`$N%@%&%s%m!<%I$b2DG=) $,MQ0U$5lF$$$k!%K\8&5fGO!$:n@.$9$k CPU $NL?Na%;%C%H%"!<%-%F%/%A%c$r KITE CPU $HF1$8K9k3HG!$$3li$N%/%m%9%=%U%H%&%'%"$rMxMQG-$k!%

3.2 KITE %^%$%/%m%W%m%;%C%5$N%"!<%-%F%/%A%c

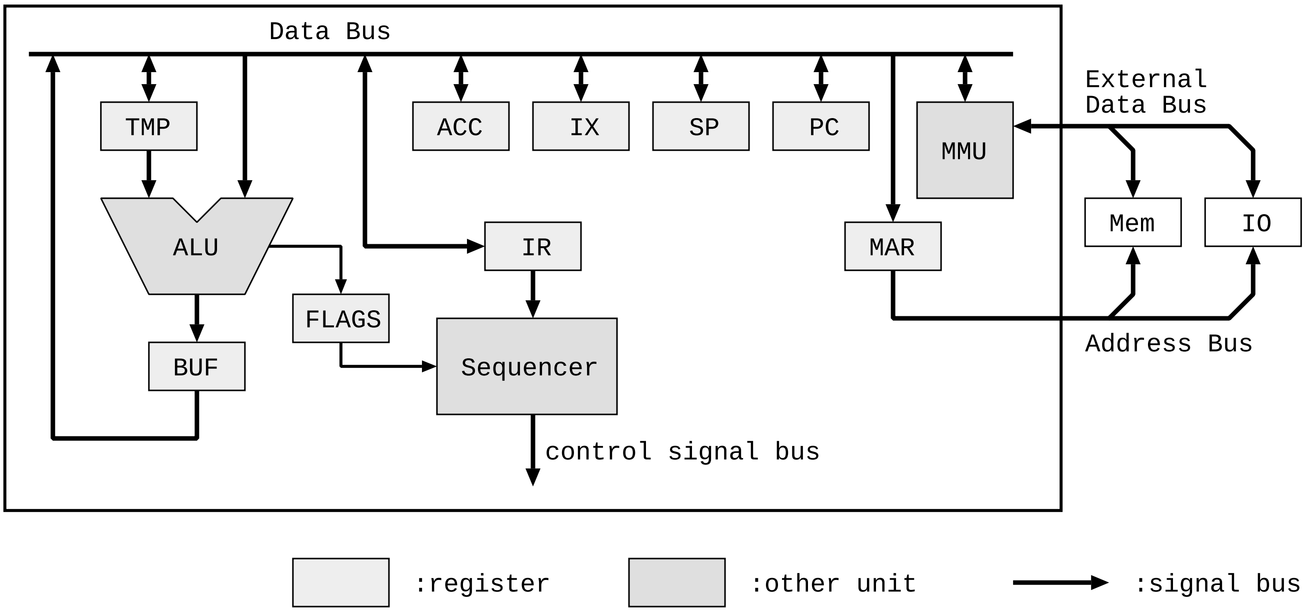
KITE %^%$%/%m%W%m%;%C%5$O!$KITE %\!<%IMQ$K@_7W5l$?650iMQ CPU G"$j!$@_7W!&<BAu$r9MN8$7$?4JC1$J%"!<%-%F%/%A%c9=@.HJCF$$$k[4]!%

CPU $NFbIt9=B$$O?^4$K<($9h&$K!$Bg$-$/J,1F 4 DN%f%K%C%H$KJ,$+lk!%

- ALU

  2C8:;;$d%7%U%H1i;;!&@M}1i;;$JIN1i;;$r9T$&!%%m!<%IL?Na$d%9%H%"L?Na$JIN%"%I%l%91i;;Kb;HMQ5l$k!%

- %l%8%9%?



?^4: KITE CPU $NFbIt9=B$

- %a%b%jF~=PNO%f%K%C%H(MMU)
  %a%b%j5Z$S I/O %]!<%H$NFI$_=P$7!&=q$-9~$_$r9T$&!%

- Sequencer
  L?Na8l$r%G%3!<%I$7!$$=l>lN%f%K%C%H$K;XNa$r=P$9!%

$=$l$>$l$N%f%K%C%H$O DataBus $H8F$Plk?.9f@~$G@\B3$5lF$*$j!$%f%K%C%H4V$N%G!<%?NdjHjO9YF3$N DataBus $r2p$7$F9T$olk!%$^$? Sequencer $+$iB>$N%f%K%C%H$X@)8f?.9f$,@\B3$5lF$$$k!%

0J2<$K KITE CPU $N%"!<%-%F%/%A%c35MW$r=RYk!%

3.2.1 %S%C%HI}

KITE CPU $O%G!<%?I}16bit!$%"%I%l%9I}12bit $N%^%$%/%m%W%m%;%C%5G"$k!%%a%b%j$O!$1%o!<%I(16bit)C10L$G%"%/%;%9$5$l!$CPU $,MxMQ2DG=$J%a%b%j$O 4K %o!<%I(8192bytes) G"$k!%L?Na8lD9$O 1 %o!<%I8GDjG"$k!%

3.2.2 %l%8%9%?9=@.

KITE CPU $N%l%8%9%?9=@.$O!$I=2$Nh&KJCF$$$k!%

- %"%-%e%`%l!<%?
  %"%-%e%`%l!<%?$O!$%l%8%9%?NCfGM#0l1i;;$r9T$&3H$,$G$-$k%l%8%9%?G"$k!%$^$?!$IO %]!<%HHN%G!<%?F~=PNOKb;HMQ5l$k!%

I=2: KITE $N%l%8%9%?9=@.

%l%8%9%?L>	(>JN,L>)	bit ?t
%"%-%e%`%l!<%?	(ACC)	16bit
%$%s%G%C%/%9%l%8%9%?	(IX)	12bit
%9%?%C%/%]%$%s%?	(SP)	12bit
L?Na%]%$%s%?	(PC)	12bit
%"%I%l%9%l%8%9%?	(MAR)	12bit
L?Na%l%8%9%?	(IR)	16bit
01;~%l%8%9%?	(TMP)	16bit
ALU %P%C%U%!	(BUF)	16bit
%U%i%0%l%8%9%?	(FLAGS)	4bit

- %$%s%G%C%/%9%l%8%9%?
  %$%s%G%C%/%9%l%8%9%?$O!$%m!<%I/%9%H%"L?Na$N!$%$%s%G%C%/%9=$>~$H7F;HMQ5l$k!%

- %9%?%C%/%]%$%s%?
  %9%?%C%/%]%$%s%?$O!$%l%8%9%?BTHr$d!$%3!<%kL?Na<B9T;~$NLa$jHVCO$r5-21$9$k$?$a$N!$%9%?%C%/$H8F$Plk%a%b%jNN0h$r;X$7<(9?aN%l%8%9%?G"$k!%

- L?Na%]%$%s%?
  L?Na%]%$%s%?$O!$<!$K<B9T9Y$-L?Na8l$,3JG<5l$F$$$k%a%b%j$N%"%I%l%9$rJ];}9k!%

- %"%I%l%9%l%8%9%?
  %"%I%l%9%l%8%9%?$O!$%"%/%;%9BP>]HJ$k%a%b%j$N%"%I%l%9$r!$KITE %\!<%I$N%O!<%I%&%'%"$KDILCN9k$?$aKI,MWJ%l%8%9%?G"$k!%

- L?Na%l%8%9%?
  L?Na%l%8%9%?$O!$8=:_<B9TCf$NL?Na8l$rJ];}9k%l%8%9%?G"$k!%

- 01;~%l%8%9%?
  01;~%l%8%9%?$O!$ALU KBP7FI,MWJ2 DN%*%Z%i%s%IN&AN1 Dr5-21$9$k%l%8%9%?G"$k!%KITE CPU $O1 %P%99=@.$G$"$k$?$a!$$3Nh$&$J%l%8%9%?$,I,MW$KJk!%$^$?!$L?Na$KhCFO!$01;~E*$J%G!<%?J];}Kb;HMQ5l$k!%

- ALU %P%C%U%!
  ALU %P%C%U%!$O!$ALU $N1i;;7k2L$r01;~E*$K5-21$9$k%l%8%9%?$G$"$k!%KITE CPU $O1 %P%99=@.$G$"$k$?$a!$$3Nh$&$J%l%8%9%?$,I,MW$KJk!%

- %U%i%0%l%8%9%?
  %U%i%0%l%8%9%?$O!$1i;;L?Na$r<B9T$7$?:]$N1i;;7k2L$N>uBV$rJ];}9k!%

MAR, IR, TMP, BUF %1%8%9%?$O!$CPU $,FbItE*$K;HMQ9k%f!<%6!<KOIT2D;k$N%1%8%9%?$G$"$j!$%f!<%6!<$,3liN%1%8%9%?$rD>@\MxMQ$9k3HOG-$J$$!%

3.2.3 L?Na%;%C%H

KITE CPU $NL?Na%;%C%H$O!Bg-$/J,$1$F!$%G!<%?E>AwL?Na!$J,4tL?Na!$1i;;L?Na!$CPU @)8fL?Na $N4 <oN`$,$"$k!%I=3$KA4L?Na$N35MW$r<($9!%

I=3: KITE CPU $NL?Na0lMw

%G!<%?E>AwL?Na	LD ST MV IN OUT PUSH POP
J,4tL?Na	JP JPC JPV JPZ JPS CALL RET
1i;;L?Na	ADD SUB INC DEC OR EOR AND NOT LSL LSR ASL ASR ROL ROR SWP
CPU @)8fL?Na	NOP HALT

4 %O!<%I%&%'%"5-=R8@8lKh$k **KITE** %^%$%/%m%W%m%;%C%5 $N<B8=

4.1 %^%$%/%m%W%m%;%C%53+H/$NN.$l

VHDL $G KITE CPU $r5-=R$7!$KITE %\!<%I>e$GF0:n5;k^GNN.lr0J2<$K=R$Y$k!%$^$?!$$=$NN.$l?^$r?^5$K<($9!%

J*!$K\8&5f$G$O%3%s%Q%$%iJIH7$F0J2<$N%D!<%k$r;HMQ$7$F$$$k!%

- %7%_%e%l!<%7%g%sMQ%3%s%Q%$%i — Menter Graphics <R@=Design Architect
- FPGA MQ%3%s%Q%$%i — Menter Graphics <R@=Auto Logic II
- %O!<%I%&%'%"9=@.%G!<%?@8@.%D!<%k — Xilinx <R@=XACT

1. VHDL %=!<%9%U%!%$%k$N:n@.
   CPU $r VHDL $G5-=R$9$k!%CPU $N5-=R$ONL$,B?$/Jk$?$a!$0l$D$N%U%!%$%k$KA4%=!<%9$r=q$->e$2kN$O8=<BE*$GOJ$$!%9,$$!$VHDL $O3,AX9=B$5-=R$r%5%]!<%H$9kN$G!$%3%s%]!<%M%s%HKh$KJ,3d$7$F5-=R$7!$%7%_%e%l!<%7%g%sEy$r9T$$!$E,;~7k9g$7$F FPGA >e$GF0:n8!>Z$r9T$&!%

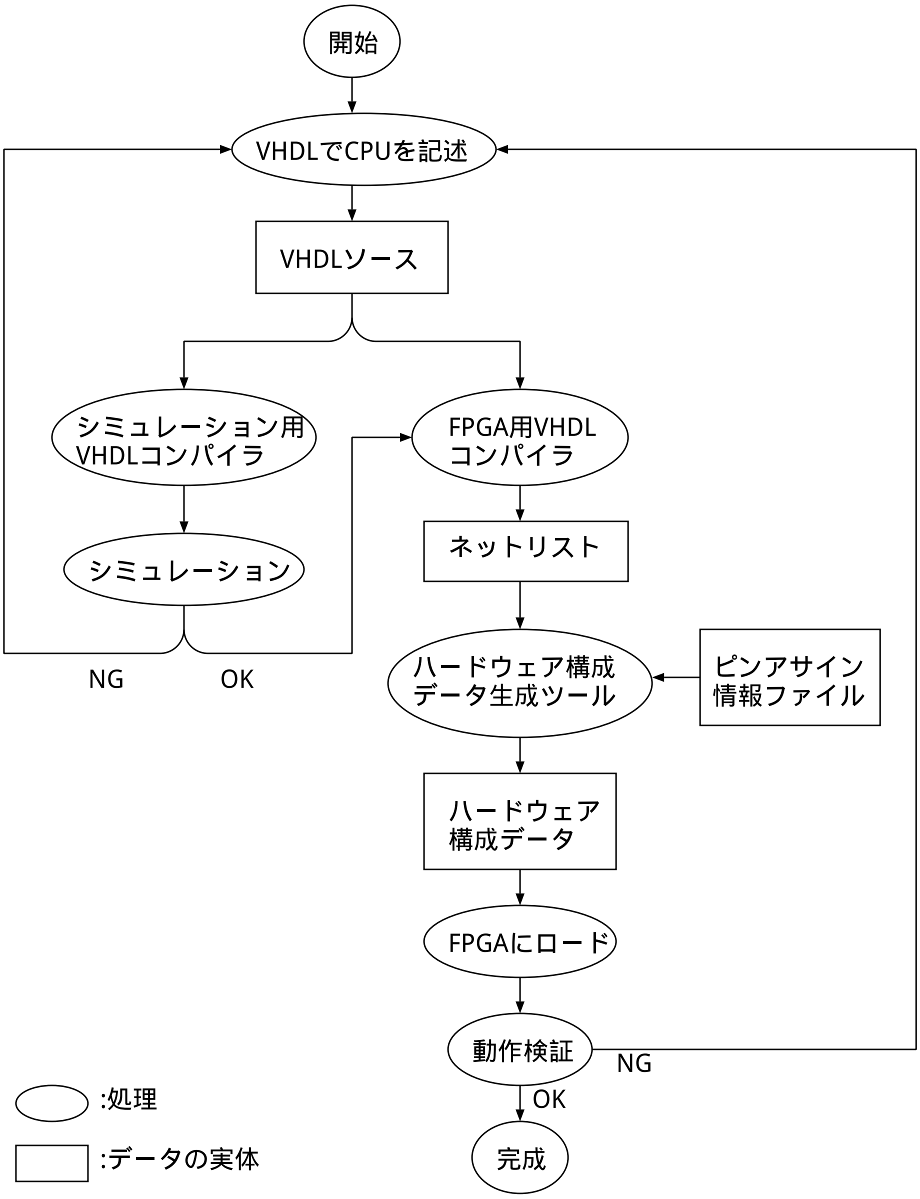
2. %7%_%e%l!<%7%g%s
   %7%_%e%l!<%7%g%sMQ VHDL %3%s%Q%$%i$G%3%s%Q%$%k$7!$%7%_%e%l!<%7%g%s$r9T$&!%%7%_%e%l!<%7%g%s7k2L$O!$%7%_%e%l!<%7%g%s%D!<%k$,=PNO7??.9f$NGH7A$G3NG'G-$k!%%7%_%e%l!<%7%g%s7k2L$,0U?^7?H*jGJ1lP!$A09)Dx$KLa$j%G%P%C%0$r9T$&!%

3. %M%C%H%j%9%H$N@8@.
   FPGA MQ VHDL %3%s%Q%$%i$G%3%s%Q%$%k$7!$%M%C%H%j%9%H$r@8@.9k!%%M%C%H%j%9%HHO!$VHDL 5-=R$r%G%P%$%9$K0MB8$7$J$$O@M}%2!<%H%l%Y%k$NO@M}2sO)$KJQ49$7$?7k2LG"$k!%$^$?F1;~$K!$O@M}2sO)$N:GE,2=$,9T$olk!%

4. %O!<%I%&%'%"9=@.%G!<%?$N@8@.
   %O!<%I%&%'%"9=@.%G!<%?@8@.%D!<%k$rMQ$$$F!$%O!<%I%&%'%"9=@.%G!<%?$r@8@.9k!%%O!<%I%&%'%"9=@.%G!<%?HO!$%G%P%$%9$K0MB8$7$J$$O@M}%2!<%H%l%Y%k$NO@M}2sO)%G!<%?$r!$%G%P%$%9FH<+$NO@M}2sO)%G!<%?$KJQ49$7$?7k2LG"$k!%

   $^$?!$VHDL Fb$NO@M}E*$J?.9fL>$H FPGA $NJ*M}E*$J%T%sHN4XO"IU1b!$$3$N;~$K9Tol$k!%$3$N>pJs$r5-=R7?!V%T%s%"%5%$%s>pJs%U%!%$%k!Wr"i+8aMQ0U7F$*$+J1lPJi$J$$!%

5. FPGA >eGNF0:n3NG'
   %O!<%I%&%'%"9=@.%G!<%?$r FPGA $K%@%&%s%m!<%I$7$FF0:n8!>Z$r9T$&!%%a%b%j%"%/%;%9$J$I!$KITE %\!<%I$N%O!<%I%&%'%"$r;HMQ9k%3%s%]!<%M%s%H$O!$%7%_%e%l!<%7%g%s$@$1GOF0:n3NG'$,$G$-$J$$$?$a!$$3$N;~$K8!>Z9k3HKJ$k!%



?^5: KITE CPU 3+H/$NN.$1

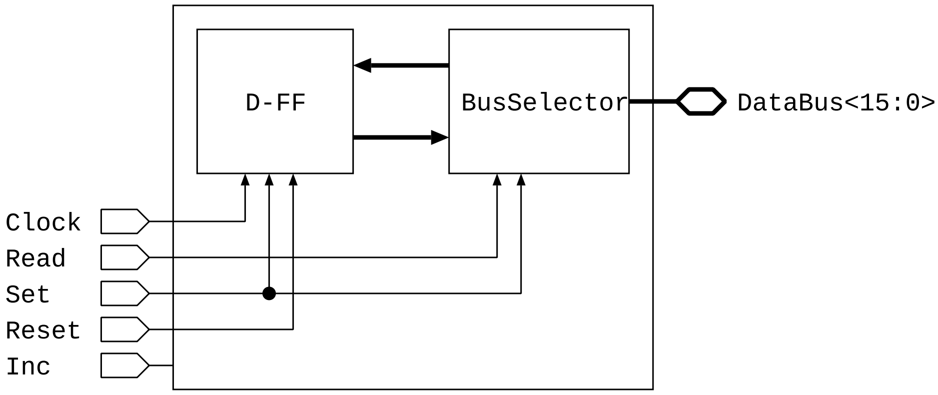
4.2 %G!<%?%P%9$N9=@.

KITE CPU GO!$?^4$K<(9H$*$j!$3F%f%K%C%H$O%G!<%?%P%9(DataBus)$K@\B3$5lF$*$j!$%f%K%C%H4V$N%G!<%?Nd$j<h$jO9YF3N%G!<%?%P%9rDL8$F9T$olk!%7+$7!$$9YF$N%f%K%C%H$,>o$K%G!<%?%P%9$K%G!<%?$rN.$7B3$1$F$$$?NG$O!$6q9g$,0-$$!%%G!<%?$rF I$_=P7?$$%f%K%C%H$@$1$rA*Br$7$F!$%G!<%?%P%9$K%G!<%?$r=PNO9kI,MW$,$"$k!%

3Nh&J3Hr9T$&$K$O!$%^%k%A%W%l%/%5$rMQ$$$kJ}K!b"k,!$:#2s$O3%9%F!<%H%P%C%U%!$rMQ$$$k3HK7$?!%3%9%F!<%H%P%C%U%!$rMQ$$$k$H!$%^%k%A%W%l%/%5$rMQ$$$kJ}K!hj$b!$O@M}%2!<%H?t$r@aLs$G$-$k$H$$$&MxE@$,$"$k[4, 12]!%$7$?$,CF!$%G!<%?%P%9$K%G!<%?$r=PNO$9$k%f%K%C%H$O9Y$F!$3%9%F!<%H%P%C%U%!$r2p$7$F9T$olk!%

4.3 %l%8%9%?

%l%8%9%?$O!$D-Flip Flop $rMQ$$$F9=@.9k!%%l%8%9%?$N3O4Q$*hSFbIt9=B$$O?^6Nh$&$KJC$F$$$k!%



?^6: %l%8%9%?$N3O4Q$HFbIt9=B$

D-FF It$O%l%8%9%?$NCf?u$G!$D-Filp Flop $rI,MW8D?t$JiY$F!$%G!<%?$rJ];}$9$k!%BusSelector It$O3%9%F!<%H%P%C%U%!$G9=@.$5lF$*$j!$Read $^$?$O Set ?.9f$K1~8F!$D-FF $N%G!<%?$r%G!<%?%P%9$K=PNO$7$?$j!$%G!<%?%P%9$N%G!<%?$r D-FF $KN.$7$?$j9k!%

3F%]!<%H$N>\:Y$K$D$$$F@bL@9k!%

- DataBus

  CPU $N%G!<%?%P%9$K@\B3$9$k$?$a$NF~=PNO%]!<%H$G$"$k!%

- Clock

  %/%m%C%/?.9f$,6!5k$5lk!%

- Read

  Read = High NH$-!$%l%8%9%?$OJ];}$7$F$$$k%G!<%?$r DataBus %]!<%H$K=PNO9k!%

%G!<%?%P%9$O16bit G"k?$a!$12bit %1%8%9%?$,=PNO$r9T$&>l9g$O!$>e0L4bit $O>o$K0 $,=PNO$5lk!%

- Set
  Clock $NN)$A>e$,$j;~$K Set = High G"lP!$%1%8%9%?$O DataBus %]!<%H$KF~NO$5lF$$$k%G!<%?$rFbIt$KJ];}9k!%%G!<%?%P%9$O16bit G"k?$a!$12bit %1%8%9%?$,J];}$r9T$&>l9g$O!$>e0L4bit $OL5;k$5lk!%

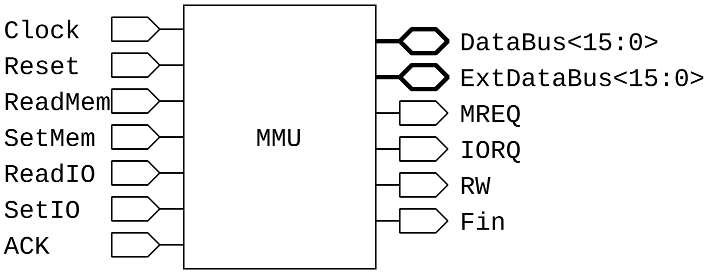
- Reset
  Reset = Low K9kH!$%1%8%9%?$O7hail?=i4 |CM$K=i4 |2=$5lk!%IaCJ$O Sequencer KhCF High K5lF$$$k!%

- Inc
  %W%m%0%i%`%+%&%s%?(PC) $@$1$,;}$D@)8f?.9fG"$k!%Clock $NN)$A>e$,$j;~$K Inc = High G"lP!$PC O=NCMr +1 9k!%

PC $N%$%s%/%j%a%s%HMQ$K!$ALU HOJL$K@lMQ$N2C;;4o$rMQ0U$7$?!%$3lO!$L?Na8l$N%U%'%C%A$KH<$&%/%m%C%/?t$r8:>/$5$;!$$^$? Sequencer $rC1=c2=$9k?aG$"$k!%

4.4 %a%b%jF~=PNO%f%K%C%H (MMU)

MMU $N304Q$O?^7Nh$&$KJC$F$$$k!%



?^7: MMU $N304Q

3F%]!<%H$N>\:Y$K$D$$$F@bL@9k!%

- DataBus
  CPU FbIt$N%G!<%?%P%9$K@\B3$9$k$?$a$NF~=PNO%]!<%H$G$"$k!%

- ExtDataBus
  CPU 30It$N%G!<%?%P%9$K@\B3$9$k$?$a$NF~=PNO%]!<%H$G$"$k!%

- Clock, Reset
  %/%m%C%/?.9f!$%j%;%C%H?.9f$,6!5k5l$k!%MMU $O%9%F!<%H%^%7%s$G$"$k$?$a!$%j%;%C%H;~$K=i4 |>uBVKLa9I,MW$,$"k?$a!$%j%;%C%H?.9f$b6!5k$5lk!%

- ReadMem, SetMem, ReadIO, SetIO
  Sequencer $+$i MMU KBP9$k!$%a%b%j/IO %"%/%;%9MW5aN?aN@)8f?.9fG"$k!% %/%m%C%/$NN)$A>e$,$j;~$K!$$3li$N@)8f?.9f$N$$$:l+$, High G"lP!$MMU $OF0:n$r3+;O9k!%
- MREQ, IORQ, RW
  MMU $+$i KITE %\!<%IKBP9$k!$%a%b%j/IO %"%/%;%9MW5a?.9fG"$k!%
- ACK
  KITE %\!<%I$+$i$N%a%b%j/ IO %"%/%;%95v2D?.9f (%"%/%N%j%C%8?.9f) G"$k!%
- Fin
  MMU $NF0:n$,40N;7?3H$r!$Sequencer $KDLCN$9k?aN?.9fG"$k!%

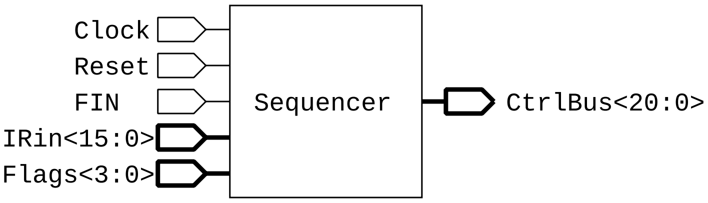
MMU $,C4$&Lr3d$O!$KITE %\!<%I>e$N%a%b%j/ IO %"%/%;%9$KI,MW$J!$MREQ, IORQ, RW ?.9f$r@)8f$7!$$^$? ACK ?.9f$r4F;k9k3HG"$k!%MREQ ?.9f$JIr ACK ?.9f $K1~$8$F@)8f$7J1lPJi$J$$$?$a!$MMU $OJ#?t$NA+0\>uBV$r;}$D%9%F!<%H%^%7%sHJCF$$$k!%

3Nh&$J5!G=$O Sequencer KAH_9~$`$3Hb2DG=G"k,!$MMU H7$F Sequencer $HJ,N%$9k3HG!$MMU $r%5%V%k!<%A%s$Nh&$J7A$GMxMQG-!$Sequencer $NA+0\>uBV?t$r8:i9$3$H$,=PMh$k!%

$^$?!$Sequencer $H MMU $N2 DN%9%F!<%H%^%7%s$,F14 |$r<hk?aK$O!$MMU $NF0:n4 0N;$r< ($9?.9f Fin $,I,MW$KJk!%

4.5 Sequencer

Sequencer $N3 04Q$O?^8Nh$&$KJC$F$$$k!%



?^8: Sequencer $N3 04Q

3F%]!<%H$N>\:Y$K$D$$$F@bL@9k!%

- Clock, Reset
  %/%m%C%/?.9f!$%j%;%C%H?.9f$,6!5k5l$k!%Sequencer $O%9%F!<%H%^%7%s$G$"$k$?$a!$%j%;%C%H;~$K=i4 |>uBVKLa9$?$a%j%;%C%H?.9f$b6!5k$5lk!%

- CtrlBus
  %1%8%9%?!&MMU !&ALU KBP9$k@)8f?.9f$r=PNO9k!%

- FIN
  MMU $+$i$NF0:n40N;?.9f$r<u$1<h$k!%

- IRin
  8=:_<B9T9Y$-L?Na8l$r5-21$7$F$$$k%$%s%9%H%i%/%7%g%s !&%1%8%9%?NCM,F~NO$5 lk!%

- Flags
  ALU $+$i$N%U%i%0$,F~NO5l$k!%>r7oJ,4tL?Na$GMxMQ5l$k!%

%a%b%jNCMr%1%8%9%?$K%m!<%I$9$k>l9g!$

1. MMU $K!$!V%a%b%jNCMr%G!<%?%P%9$K=PNO!W$9kh$&MW5a$9$k!%
2. %1%8%9%?$K!$!V%G!<%?%P%9$K=PNO$5lF$$$k%G!<%?$r<h$j9~$`!W$h$&MW5a$9$k!%

$H$$$C$?<j=g$rF'$`$3HG<B8=G-$k!%

3Nh&$K!$$=l>lN%f%K%C%H$K!$7hail?=g=x$G;XNa$r=P$9=hM}$,I,MWG"$k!%$3$N=hM}$r9T$&$N$,%7!<%1%s%5$G$"$j!$@)8f?.9f$r High K9k3HKhC$FB>$N%f%K%C%HKBP7$F;XNa$r=P$9!%

4.6 ALU

ALU $N304Q$*hSFbIt9=B$$r?^9$K<($9!%
3F%]!<%H$N>\:Y$K$D$$$F@bL@9k!%

- Op1, Op2
  1i;;KI,MWJ2 DN%*%Z%i%s%I (16bit) $,F~NO$5lk!%

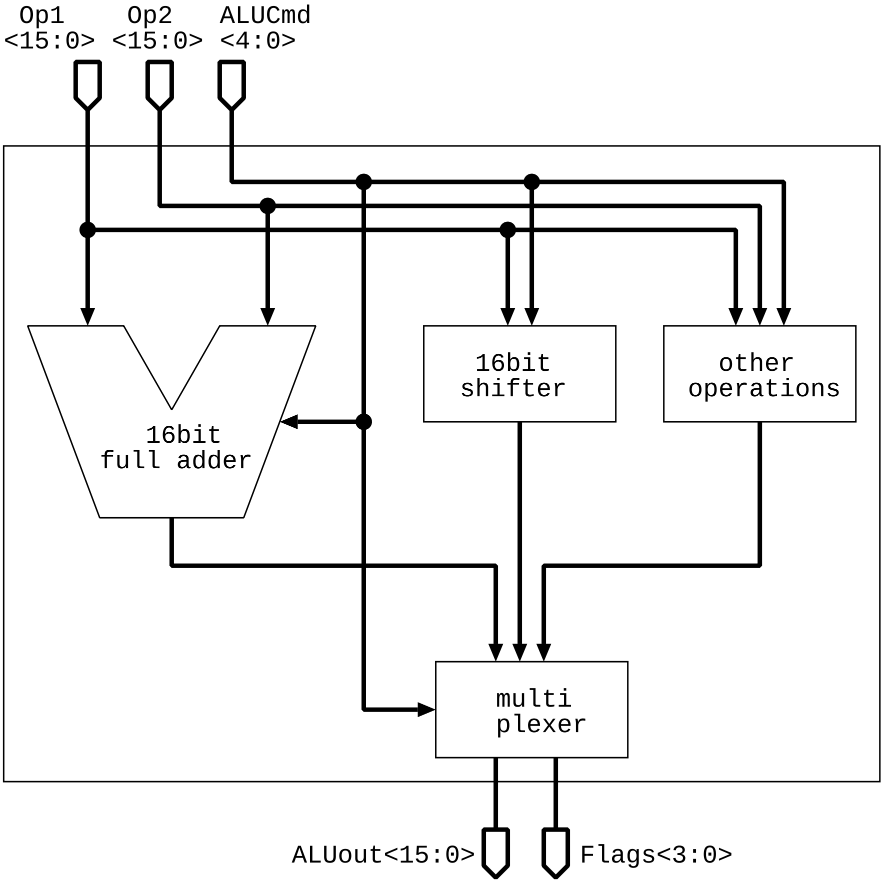
- ALUCmd
  ALU KBP7$F!$$INh$&$J1i;;$r9T$&$+$r;X<(9k?.9fG"$k!%

- ALUout
  ALU $, 16bit $N1i;;7k2L$r=PNO9k!%

- Flags
  1i;;7k2L$K1~$8$F!$ZF (%<%m%U%i%0), CY (%-%c%j!<%U%i%0), OV (%*!<%P!<%U%m!<), SF (Id9f%U%i%0) $N 4bit $N%U%i%0$r=PNO9k!%

ALU $NFbIt$O<!Nh$&$K 3 DNItJ,$KJ,$+lk!%

- 2C;;4oIt — 01DN2C;;4o$G!$2C;; (ADD) !&8:;; (SUB) !&Hf3S (CMP) $r9T$&!%



?^9: ALU $N3 04Q$*hSFbIt9=B$

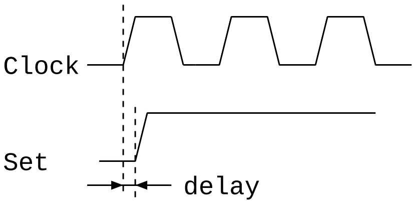
- %7%U%H1i;;It — 9YFN%S%C%H%7%U%H1i;;$r9T$&!%
- $=$NB>$N1i;; — AND, OR, XOR, NOT, NEG L?NaJI$N1i;;!%

3liNItJ,$,%^%k%A%W%l%/%5$KhCF^Hail!$ALUCmd $K1~$8$?1i;;It$,A*Br5l!$7k2L$,=PNO5l$k!%

4.7 %/%m%C%/$N>\:Y

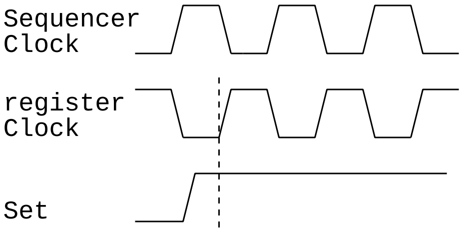
Nc$($P!$%1%8%9%?$K%G!<%?$r%;%C%H$7$?$$>l9g!$%7!<%1%s%5$O Clock $NN)$A>e$,$j$G Set $r High K9$k!%7+$7!$?^10$Nh&$K!$O@M}2sO)$NEAGECY1d$JIKhC$F!$Set $NJQ2=$, Clock hjbCYl$?>l9g!$%1%8%9%?B&GO Clock $NN)$A>e$,$j;~KO Set O^$@ Low N^$^$JNG!$%1%8%9%?$O%G!<%?$r%;%C%H7J$$!%9JoA!$Sequencer $,%1%8%9%?$KBP7F%G!<%?$r%;%C%H$9kh$&MW5a$7$?$Kb+$+$oi:!$%1%8%9%?$K$O%G!<%?$,%;%C%H5l$J$$H$$$&LdBj$,5/$3$k!%

3l$r2sHr$9kK$O!$Set $,4 0A4$K High $K3ND j$7F+$i!$%1%8%9%?$K6!5k$9$k Clock $r Low "* High $KJQ2=$5$;$kI,MW$,$"$k!%



?^10: %l%8%9%?$H Sequencer $KF1$8%/%m%C%/$r6!5k$7$?>l9g

$=$3$G!$?^11Nh$&$K!$%l%8%9%?$K$O!$Sequencer $HH>0LAj$:l? Clock $r6!5k$9$k!%$3$&$9lP!$Sequencer $, Set $r High K7$?H>%/%m%C%/8e$K%l%8%9%?$N Clock $, Low "* High $KJQ2=$9kN$G!$$3Nh$&$JLdBj$r2sHr$G$-$k!%

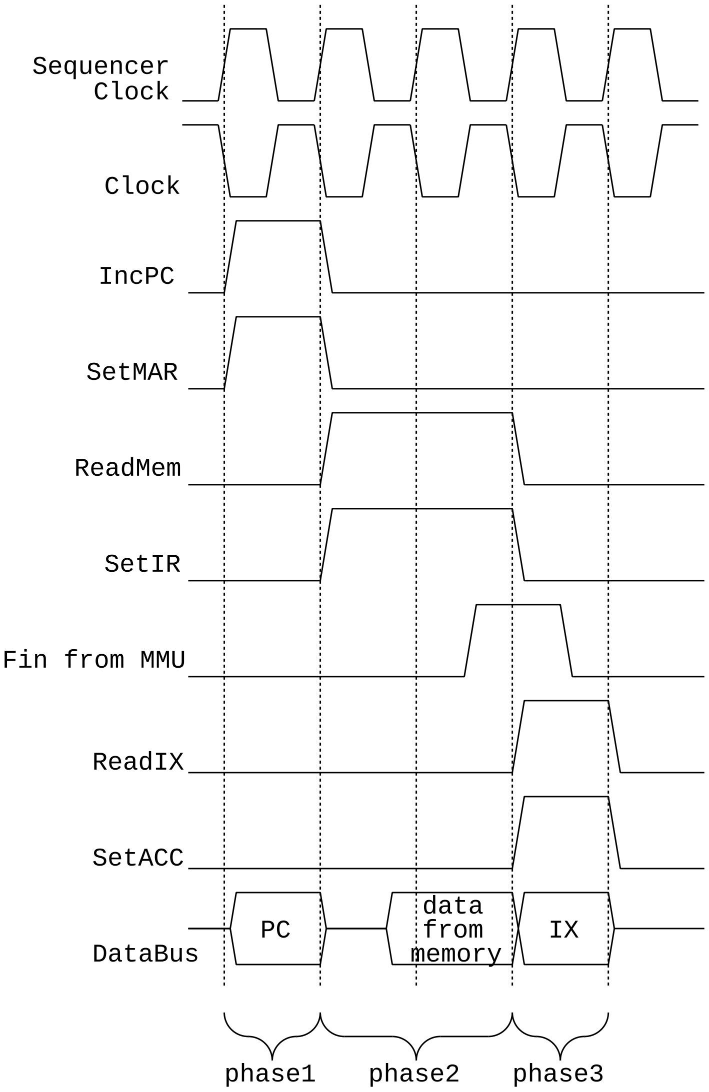


?^11: %l%8%9%?$K Sequencer $HH>0LAj$:l?%/%m%C%/$r6!5k$7$?>l9g

F1MM$NM}M3$+$i!$Sequencer 0J30$N%f%K%C%H$K6!5k9k%/%m%C%/$O Sequencer $K6!5k$9$k%/%m%C%/$H$OH>0LAj$:l?%/%m%C%/$r6!5k$9$k!%

NcH7$F!$"MV ACC,IX" L?Na(IX NCMr ACC $KBeF~) $,<B9T$5lkH-$N3F?.9f$NMM;R$r?^12$K<($9!%

1. Bh1 %U%'%$%:— MAR $N%;%C%H
   %"%/%;%9BP>]H9$k%a%b%j$N%"%I%l%9$r!$PC $,;X$9%"%I%l%9K9k?$a!$PC NCMr MAR $KBeF~$9$k!%SeqClock $NN)$A>e$,$j$G!$Sequencer $O IncPC $H SetMAR $r High K9$k!%IncPC $, High K5lk3H$G!$PC NCM,%G!<%?%P%9$K=PNO$5lk!%$=7F!$Clock $NN)$A>e$,$j(SeqClock $NN)$A2<$,$j) $G!$MAR $O%G!<%?%P%9$K>hCF$$$k PC NCMrFbIt$KJ];}$9$k!%$5iK!$PC O=NCMr +1 9k!%
2. Bh2 %U%'%$%:— L?Na8l$N%U%'%C%A
   %a%b%j>e$NL?Na8l$r IR $K%;%C%H$9k?aK!$Sequencer $O ReadMem $H SetIR $r High K9$k!%ReadMem $, High K5lk3H$G!$MMU $O%a%b%j$NCM$r%G!<%?%P%9$K=PNO9Y$/F0:n$r3+;O9k!%SeqClock $NN)$A>e$,$j;~$K Fin = High G"lP!$Sequencer $OBh2 %U%'%$%:$+$iBh3 %U%'%$%:$X0\9T9k!%
3. Bh3 %U%'%$%:— L?Na<B9T
   L?Na8l$, IR $KF~$k$HF1;~$K!$Sequencer KhCFL?Na8l$,%G%3!<%I$5lk!%$=7F!$



?^12: “MV ACC,IX” <B9T;~$N3F?.9f$NMM;R

IX NCMr ACC $KBeF~$9k?aK!$ReadIX $H SetACC $r High K9$k!%Clock $N N)$A>e$,$j$G ACC $O IX NCMrFbIt$KJ];}9k!%

J*!$KITE CPU KO!$DVL>oF0:n!W!1V%/%m%C%/F0:n!W!1V L?NaF0:n!W$N3 DN%/%m%C%/%b!<%I$,$"k,!$$3li$N5!G=$O!$$9YF KITE %\!<%IB&$N5!G=$G$"$kNG!$$3li$N5!G=$rMxMQ9k$?$a$K KITE CPU B&$G<BAu9Y$-5!G=$O$J$$!%

5 F0:n8!>Z

F0:n8!>Z$r9T$&KO!$<B:]$K FPGA >e$GF0:n$5$;$kJ}K!N[$+!$%7%_%e%l!<%7%g%sKhCF$b9T$&3H$,$G$-$k!%8!>ZJ}K!H7FO!$F~NO$5l?CMKBP7$F4|BT$5lk7k2L$,F@$ilk$+$r!$2?2s$b7+jJV9$[$+$J$$!%

<B:]$KF0:n8!>Z$r9T$&$K$O!$3F%f%K%C%H$N<BAu=g=x$,=EMWKJCF$/$k!%K\8&5fGO!$%\%H%`%"%C%WJ}<0$G!$%l%8%9%?"*MMU "*Sequencer "*ALU $N=g$K:n@.$9$k$3$H$K$9$k!%F%9%H$9$Y$-9`L\$d!$%F%9%HCf$KH/8+5l$?LdBjE@$JIr0J2<$K=R$Y$k!%$J$*!$K\8&5fGO§5.4 $^$G7+40N;7F$*$i$:!$§5.5 0J9_$O%F%9%H$9Y-9`L\$N$_$r=RYk!%

5.1 %l%8%9%?$N%F%9%H

$^$:O8aK!$%l%8%9%?$r:n@.$7!$%7%_%e%l!<%7%g%s8e$K!$FPGA $GF0:n8!>Z$r9T$&!%

- 8!>ZFbMF
  1. Clock $NN)$A>e$,$j;~$K DataBus $N%G!<%?$,FbIt$KJ];}$5lk$+$I$&$+!$$^$?!$$=$l0J30$NH-$K DataBus NCMrJQ99$7FbJ];}$5lF$$$kCM$KJQ2=$,$J$$$+I&$+
  2. %j%;%C%H;~$K7h$ail$?=i4|CM$K=i4|2=5lk+I&$+
- H/8+5l$?LdBjE@$HBP:v

  FC$K!$LdBjOJ$+$C$?!%

5.2 MMU $N%F%9%H

MMU $r:n@.$7!$%7%_%e%l!<%7%g%s$r9T$&!%MMU $O KITE %\!<%I$N%O!<%I%&%'%"$K%"%/%;%9$9$kItJ,$JNG!$%7%_%e%l!<%7%g%s$@1G$O40A4$K@5Ev@-$r8!>Z$9k3HOG-$J$$$,!$%9%F!<%H%^%7%s$N>uBVA+0\$N3NG'$r9T$&!%

- 8!>ZFbMF

  ReadMem $d SetIO Ey$NL?NaKBP7$F!$@5$7$$=g=x$G MREQ, IOREQ, RW ?.9f$r Aw=P7F$$$k$+$I$&$+$N3NG'

- H/8+5l$?LdBjE@$HBP:v

  ReadMem JI$NL?Na$KBP9kF0:n$,40N;$7$?D>8e$K!$F1$8L?Na$N<B9T$r;X<(9k$H!$%9%F!<%H%^%7%s$,L58B%k!<%W$K4Y$kLdBj$,H/@8$7$?!%3l$O!$A+0\>uBV$r=$@5$9$k3H$G2sHr$7$?!%

5.3 Sequencer $N%F%9%H

Sequencer $N0lIt$N5!G=$r:n@.$7!$%7%_%e%l!<%7%g%s$r9T$&!%$3$N Sequencer $OL?Na%G%3!<%I5!G=$r;}$?$:!$%l%8%9%?$*hS MMU $N%G!<%?E>Aw$r@)8f9k$@$1$N5!G=$r;}$D!%$3Nh$&$J2>$N Sequencer $r:n@.$9$kL\E*$O!$%7%_%e%l!<%7%g%s$@1G$O8!>Z$7$-$l$J$$MMU $r FPGA >e$G8!>ZF0:n9k$?$aG"$k!%

- 8!>ZFbMF

  %/%m%C%/$NN)$A>e$,$jKh$K!$@5$7$$@)8f?.9f$rAw=P$7$F$$$k$+$I$&$+

- H/8+5l$?LdBjE@$HBP:v

  FC$K!$LdBjOJ$+$C$?!%

5.4 %a%b%j%"%/%;%9/%l%8%9%?%G!<%?E>Aw$N%F%9%H

Sequencer + %l%8%9%? + MMU $r FPGA >e$G%F%9%H$r9T$&!%3N%F%9%H$r%/%j%"$9lP!$L?Na8l$N%U%'%C%A!$%m!<%I/%9%H%"L?Na$JIN!$CPU $N4pK\F0:n$@1O<B9TG-k3HKJk!%9JoA!"L?Na8l$N%U%'%C%A"*%G%3!<%I"*(8Bil$?) L?Na$N<B9T!W$H$$$& CPU $N4pK\%5%$%/%k$r4 0@.$5$;$k3H$,$G$-$k!%

- 8!>ZFbMF

  1. MMU $, KITE %\!<%I$N%O!<%I%&%'%">e$G@5$7$/F0:n$9k+
  2. Sequencer $,@5$7$/@)8f?.9f$rAw=P$7!$B>$N%f%K%C%H$r@)8f7F$$$k$+$I$&$+
  3. J#?t$N%f%K%C%H$,%G!<%?%P%9$K@\B3$5lF$$$k>uBV$G!$3 %9%F!<%H%P%C%U%!KhCFL\E*$N%f%K%C%H$N%G!<%?$@$1$,=PNO$5lF$$$k$+$I$&$+

- H/8+5l$?LdBjE@$HBP:v

  1. IO %"%/%;%9;~$K ACK ?.9f$,JVCF3:$K!$CPU $,$=3GDd;_9k$H$$$&LdBj$,$"C?!%IO %"%/%;%9;~KO%"%I%l%9%P%9NCMO4X78$J$$$H;WCF$$$?N@$,!$<B:]$O%"%I%l%9%P%9$, 000h GJ$$$H ACK $,JV$CF3$J$$$H$$$&;EMMG"C?$?$a!$IO %"%/%;%9;~$K$O MAR $r 000h $K%;%C%H$9kh$&$K7?!%
  2. %/%m%C%/<~GH?t$r9b$/9k$H%l%8%9%?$NCM$,IT@5$JCMKJk3H,$"$C$?!%$=3G §4.7 $G=R$Y$?BP:v$r9TC?!%

5.5 ALU $N%F%9%H

ALU $r:n@.$7!$%7%_%e%l!<%7%g%s8e$K FPGA >e$G%F%9%H$r9T$&!%

- 8!>ZFbMF

  M?$($il? 2 DN%*%Z%i%s%I$,!$;XDj5l$?1i;;L?Na$KhC$F@5$7$$CM$r=PNO$9k+I&$+!%%U%i%0$N7k2LKbCm0U7J1lPJiJ$$!%

5.6 A4%f%K%C%H$N%F%9%H

Sequencer + ALU + %1%8%9%? + MMU $r FPGA >e$G%F%9%H9k!%3N;~E@$G!$CPU $NA4%f%K%C%H$N<BAu$,=*$oC?NG!$8e$O Sequencer $NL?Na%G%3!<%I$t$r3HD%$7!$L?Na$rDI2C7F$$$/$@$1G"$k!%E,;~ FPGA >e$G%F%9%H$r9T$$!$$9YF$N5!G=$N<BAu$,=*N;$9lP40@.G"$k!%

- 8!>ZFbMF
  3N;~E@$G!$L$<BAu$NL?Na$r=|$-DI>o$N KITE CPU H7$F2TF0$9kN$G!$%"%;%s%V%iKh$j($^$?$O<jF0$G) %F%9%H7?$$L?Na$N%3!<%I$r@8@.$7!$<B9T5;$F7k2L$r3NG'9k!%

5.7 40@.8e$N%F%9%H

40@.8e$O!$KITE CPU MQK"i+8aMQ0U5l$?%3%s%Q%$%i/%"%;%s%V%i$rMQ$$$F%W%m%0%i%`$r:n@.$7!$KITE %\!<%I>e$K$"$i$+$8$aMQ0U$5lF$$$k KITE CPU (§3.1 ;2>H) $H:#2s:n@.$7$? KITE CPU HNF0:nHf3S$r9T$&!%

- 8!>ZFbMF
  4{B8$N KITE CPU $H:#2s:n@.$7$? KITE CPU HNF0:nHf3S$r9T$$!$8_49@-$N%F%9%H$r9T$&!%

6 $*$ojK

K\8&5fGOKITE CPU $N<B8=J}K!$K$D$$$F=R$Y!$VHDL $GKITE CPU $r@_7W$9kH6&$K!$@_7W7?CPU $r<B:]$KFPGA >e$GF0:n$5$;!$8!>Z$r9T$C$?!%

8=;~E@GO!$%l%8%9%?$HMMU $O40@.$7!$Sequencer $O0lIt40@.!$ALU KD$$$F$OVHDL GN5-=Rr[$\=*$(!$%7%_%e%l!<%?$Khj%G%P%C%0CfG"$k!%$=$N7k2L!$CPU $O40@.$K$O;j$C$F$$$J$$$,!$FPGA >e$G!V?Na8l$N%U%'%C%A"*%G%3!<%I"*(8B$il?)L?Na$N<B9T!W$H$$$C$?CPU $N4pK\F0:n$r9T$&$bN,40@.7?!%

FPGA >eGNF0:n8!>Z$GH/8+$5l?LdBjE@JI$r9nI~$9k3HKhC$F!$CPU @_7W$N%N%&%O%&$r2qF@G-!$VHDL $HFPGA $NM}2r$H$$$&L\E*$bC#@.$5l?$H;W$olk!%:#8e$O!$Bh0lK3$NCPU $r40@.$5$;$k3H$rL\I8$K9k!%

:#2s$ON}=,E*MWAG$,6/$/!$:n@.7?CPU $O@-G=$rA4$/L5;k$7$?$bN@C?!%$=$3$G:#8e$O!$FH<+$NL?Na%;%C%H%"!<%-%F%/%A%c$r;}$A!$%2!<%H?t$d=hM}%9%T!<%IJI$b9MN8$KF~l?%*%j%8%J%k$NCPU $r@_7W$7!$$^$?!$$=$NCPU MQ$N%3%s%Q%$%i/%"%;%s%V%i$JIN%=%U%H%&%'%"$r<+F0@8@.$9$k5;=Q$K$D$$$F$b9M$($k!$$H$$$C$?J}LL$+iNHW/SW %3%G%6%$%s8&5f$r9T$$$?$$$H;W$&!%

<UK-

K\8&5f$K4X$7$F5.=E$J=u8@!$$4;XF3$r$$$?$@$-$^$7$?;3:j>!9065<x$K?<?S$N46<U$rI=$7
$^$9!%

$^$?!$?t!9$N5.=E$J=u8@$r$$$?$@$-$^$7$?>eEhL@;a!$Tran So Cong ;a$K46<U$$$?7^$9!%

;29MJ88%

[1] D9C+@nM563: VHDL Kh$k%O!<%I%&%'%"@_7WF~Lg!$CQ=PHG<R!$Feb.1995

[2] J.Bhasker: A VHDL Primer VHDL 8@81F~Lg!$CQ=PHG<R!$Oct.1991

[3] KITE %^%$%/%m%W%m%;%C%5%\!<%I PLUS+ <h07@bL@=q Version1.00!$6e=#7WB,4o3t<02q<R!$Apr.1995

[4] KITE %^%$%/%m%W%m%;%C%5%j%U%!%l%s%9!&%^%K%e%"%k Version1.00!$6e=#7WB,4o3t<02q<R!$1993

[5] %[%9%H%$%s%?!<%U%'!<%9%\!<%I<h07@bL@=q(Ver.1.00)!$6e=#7WB,4o3t<02q<R!$Mar.1995

[6] KITE %^%$%/%m%W%m%;%C%5!&%/%m%9%=%U%H%&%'%"%f!<%6!<%:!&%^%K%e%"%k Version 2.0(;CDjHG)!$6e=#7WB,4o3t<02q<R!$Aug.1995

[7] :#0f@5<#,>>1JM42p,0B1:42?M>pJs=hM} Vol.36 No.7!$>pJs=hM}3X2q!$Jul.1995

[8] J.Staunstrup,W.Wolf(Eds.):Harduare/Software Co-Design!$Kluwer Academic Publishers!$1997

[9] JBLZ1Q><!$A0EDL@H~!$5\Hx@5Bg: %G%#%8%?%k2sO)$H Verilog-HDL!$5;=QI>O@<R!$1996

[10] Cf9,@/:%H%i%s%8%9%?5;=Q12!$VHDL Kh$k%m%8%C%/@_7WF~Lg!$CQ=PHG<R!$Dec.1997

[11] B<2,MN01,@P0f5HI':CAD Kh$k%^%$%/%m!&%W%m%;%C%5$N@_7W!$%5%$%(%s%9<R!$Apr.1995

[12] 0B1:42?M>pJs2J3XN?aN650iMQ%^%$%/%m%W%m%;%C%5%7%9%F%`$N3+H/!$6e=#Bg3XAm9gM}9)3X8&5f2J!$Mar.1996